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EXAMINER	
KROFCHECK, MICHAEL C	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action

1. The proposed response filed on 6/3/2008 has been entered because there are no amendments to the claims included.

Response to Arguments

2. Applicant's arguments filed 6/3/2008 have been fully considered but they are not persuasive.

3. Applicant argues with respect to claim 1 that the examiner's interpretation of "synchronization signals" is improper and does not take into account the synchronization signals recited in the specification. The examiner disagrees.

The applicant indicates page 3, lines 8-15, page 4, line 24-25, and page 5, line 7-16 as where the specification describes the meaning of "synchronization signals." Yet those paragraphs talk of a "synchronization data stream," that contains "required data transitions" (specification, page 3, lines 8-15), that "synchronization cycles" may be required (page 4, line 24-25) and that other "DoSynch" signals trigger synchronizations signals "when needed" (page 5, lines 7-16). Nowhere in the specification is there an explicit definition defining what "synchronization signals" means. If the examiner were to include additional limitations in the claims from the specification when they are not explicitly recited in the claims, this would violate MPEP 2111.01 II which states:

> "Though understanding the claim language may be aided by explanations contained in the written description, it is important not to import into a claim limitations that are not part of the claim. For example, a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment." Superguide Corp. v. DirecTV Enterprises, Inc., 358 F.3d 870, 875, 69

USPQ2d 1865, 1868 (Fed. Cir. 2004). See also Liebel-Flarsheim Co. v. Medrad Inc., 358 F.3d 898, 906, 69 USPQ2d 1801, 1807 (Fed. Cir. 2004)

4. Applicant argues with respect to claim 1 that Bashirullah does not teach of the synchronization signal being transmitted "responsive to the achieved transition density." The examiner disagrees.

Bashirullah paragraph 57, 29-61 teach of the transition detectors detecting a change in the input data bits which is a change in the transition density, resulting in the assertion of a control signal. The control signal causes the repeaters to switch to current mode and propagates the data bits to the output. The data bits are the synchronization signal in this case and they are propagated in current mode resulting from the detection of the transition density changing. Additionally in paragraph 60, when there are no transitions within Cp, control signals indicate to switch back to voltage mode. The control signals being the synchronization signals.

5. Applicant also argues the examiner's interpretation of a data lane being made up of the data bit's line and its corresponding control line indicating that it is unreasonable to interpret a data lane as including a control signal lane. The examiner disagrees.

The applicant's specification does not provide for a definition of a "data lane." The portions of the specification indicated by the applicant on page 8 of the remarks filed on 6/3/2008 merely indicate situations involving data lanes, but does not describe what constitutes a data lane. An example of a data lane definition could be: A data lane is a circuit that only carries one bit of data at a time. As there is no explicit definition of a data lane in the applicant's specification, turning to the "American Heritage College Dictionary" we see that data is defined as "numerical or other information represented in

a form suitable for computer processing." Thus, the control bits of Bashirullah (fig. 4, paragraph 58) are considered data since they used in a computer for processing. Since the Din bits and their respective control bits are data, each Din line and its control line can be considered a data line.

The applicant further states in the remarks on page 8 that a data lane is described in the above sections of the specifications as "a subset of a multi-bit data path." Bashirullah satisfies this. Figure 4 and paragraph 58 indicate that each of the Din [0:N] has a dedicated control signal generator and control signal line. Clearly the Din[0] and its control line are a part of the multi-bit path that includes all of Din [0:N] and their control lines.

6. Applicant argues with respect to claims 5 and 14 that Bashirullah does not teach of the synchronization signal being transmitted when the transition density is less than the desired density, the threshold being one transition in Bashirullah. Arguing that since the transition density is less than one, no transitions are transmitted, a synchronization signal cannot be transmitted. The examiner disagrees.

As written in claims 5 and 14, the claims state, "…at least one transition detection circuit configured to detect whether an achieved data transition density on at least one data lane is less than a desired data transition density for the at least one data lane; and a transition generator configured to transmit a synchronization signal on the at least one data lane if the achieved transition density is less than the desired data transition density…" In the claim, if the current density is less than the desired density, then the synchronization signal is transmitted. The claim does not recite anything about the

transition density during or after the transmission of the synchronization signal as the applicant appears to be arguing. The zero transition density of Bashirullah being below the threshold density of one causes the control signal (synchronization signal) to switch the operation to voltage mode (paragraphs 58, 60). The zero transition density does not signify that a transmission signal is not sent. The zero transition density causes the control signal (synchronization signal) to occur after the zero transition density is detected.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL C. KROFCHECK whose telephone number is (571)272-8193. The examiner can normally be reached on Monday - Friday.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MICHAEL C KROFCHECK/
Examiner, Art Unit 2186

/Matt Kim/
Supervisory Patent Examiner, Art Unit 2186

Michael C. Krofcheck